Claims:

1. The use of forward error correction data in a signal carried over a backplane.

2. The use of forward error correction data in a signal carried over a link between two ICS (Integrated Circuits).

3. The use of forward error correction data as defined in claim 2, wherein the two ICS are on a same circuit pack.

4. An apparatus suitable for generating a signal for transmission over a link between two ICs, said apparatus comprising:
   a) an input for receiving an input signal comprising payload data to be transmitted over the link between two ICs;
   b) a processing unit coupled to said input, said processing unit being operative for:
      i) processing the payload data in the input signal to derive forward error correction data at least in part on the basis of the payload data in the input signal;
      ii) generating an output signal comprising the payload data received in the input signal and the forward error correction data generated in i);
   c) an output for releasing the output signal for transmission over a link between two ICs.

5. An apparatus as defined in claim 4, wherein the link between two ICs includes a backplane portion.

6. An apparatus as defined in claim 4, wherein said processing unit is operative to apply BCH-1 coding on the payload data to derive the forward error correction data.

7. An apparatus as defined in claim 4, said processing unit being further operative for:

a) processing the input signal to generate N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data and the second portion including forward error correction data derived from the payload data in the first portion of the primary data structure;

b) bit-multiplexing the N primary data structures generated in a) to derive a compound data structure;

c) generating a frame at least in part by grouping a plurality of compound data structures generated in b);

d) generating the output signal at least in part on the basis of the frame generated in c).

~~8.~~ An apparatus suitable for generating an output signal for transmission over a link between two ICs, said apparatus comprising:

a) an input for receiving an input signal comprising data to be transmitted over the link between two ICs;

b) a processing unit coupled to said input for processing the input signal to generate an output signal in which the data is organized into a sequence of frames, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead

information, said compound data structure being derived by bit-multiplexing a set of N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion;

c) an output for releasing the output signal for transmission over a link between two ICs.

9. A method for generating a signal for transmission over a link between two ICs, said method comprising:

a) receiving an input signal comprising payload data to be transmitted over the link between two ICs;

b) processing the data in the input signal to derive forward error correction data at least on part on the basis of the payload data in the input signal;

c) generating an output signal comprising the payload data received in the input signal and the forward error correction data;

d) releasing the output signal for transmission over the link between two ICs.

10. A method as defined in claim 9, wherein the link between two ICs includes a backplane portion.

11. A method as defined in claim 9, wherein forward error correction data is derived at least in part by applying BCH-1 coding on the payload data.

12. A method as defined in claim 9, said method further comprising:

a) processing the input signal to generate N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the payload data in the first portion of the primary data structure;

b) bit-multiplexing the N primary data structures to derive a compound data structure, the compound data structure being suitable for carrying payload data and overhead information;

c) generating a frame at least in part by grouping a plurality of compound data structures;

d) generating the output signal at least in part on the basis of the frame generated in c).

~~13.~~ A method for generating an output signal for transmission over a link between two ICs, said method comprising:

a) receiving an input signal comprising data to be transmitted over the link between two ICs;

b) processing the input signal to generate an output signal in which the data is organized into a sequence of frames, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead information, said compound data structure being derived by bit-multiplexing a set of N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second

portion including forward error correction data derived from the data elements in the first portion;

c) releasing the output signal for transmission over a link between two ICs.

14. A signal carried over a carrier medium, the carrier medium comprising a link between two ICs, the signal including a sequence of frames, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead information, said compound data structure being derived by bit-multiplexing a set of N primary data structures, each primary data structure comprising a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion.

15. A signal as defined in claim 14, wherein the link between two ICS is between two ICs on a same circuit pack.

16. A signal as defined in claim 14, wherein the link between two ICS includes a backplane portion.

17. A signal as defined in claim 14, wherein N is about 4.

18. A signal as defined in claim 14, said signal having a rate of about 2.5 Gb/s.

19. A signal as defined in claim 14, wherein each frame includes 66 sequential blocks and a framing pattern.

20. A signal as defined in claim 19, wherein each primary data structure includes about 1176 bits.

21. A signal as defined in claim 20, wherein at least part of the first 1164 bits of each primary data structure includes payload data, and 12 bits include forward error correction data.

22. A signal as defined in claim 14, wherein the forward error correction data in a given primary data structure are derived by applying BCH-1 coding on at least part of the payload data of the given primary data structure.